Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Original): A method of controlling a power saving operation for a phase comparator unit, comprising the steps of:

dividing a frequency of a reference signal to generate a reference frequency divided signal;

dividing a frequency of an input signal to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal;

comparing the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result;

generating a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal;

generating a first initializing signal for initializing the output of the step of dividing the frequency of the reference signal in accordance with the power saving state canceling signal; and

generating a second initializing signal for initializing the output of the step of dividing the frequency of the input signal in accordance with ~~30~~ the power saving state canceling signal.

Claim 2 (Original): The method as claimed in claim 1,

wherein frequency dividing rates used in the step of dividing the frequency of the reference signal and in the step of dividing the frequency of the input signal can be set independently of each other.

Claim 3 (Original): A power saving operation control circuit for a phase comparator unit, comprising:

a reference signal frequency dividing unit which divides a frequency of a reference signal to generate a reference frequency divided signal;

a comparison signal dividing unit which divides a frequency of an input signal to generate a comparison frequency divided signal whose phase is to be compared with a phase of the reference frequency divided signal;

a phase comparator which compares phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result;

a canceling signal generator which generates a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal;

a first initializing signal generator which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and

a second initializing signal generator which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving state canceling signal.

Claim 4 (Original): The power saving operation control circuit as claimed in claim 3, wherein frequency dividing rates used in the reference signal frequency dividing unit and in the comparison signal frequency dividing unit can be set independently of each other.

Claim 5 (Original): A PLL frequency synthesizer comprising:

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a phase comparator unit;

a loop filter which receives an output of the phase comparator unit; and

a voltage control oscillator which receives an output of the loop filter,

the phase comparator unit comprising:

a reference signal frequency dividing unit which divides a frequency of a reference signal to generate a reference frequency divided signal;

a comparison signal dividing unit which divides a frequency of an output signal of the voltage control oscillator to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal;

a phase comparator which compares the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result;

a canceling signal generator which generates a power saving state canceling signal in accordance with the reference frequency divided 35 signal and the comparison frequency divided signal;

a first initializing signal generator which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and

a second initializing signal generator which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving state canceling signal.

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Claim 6 (Original): The PLL frequency synthesizer as claimed in claim 5, wherein frequency dividing rates used in the reference signal frequency dividing unit and in the comparison signal frequency dividing unit can be set independently of each other.

Claim 7 (Original): A semiconductor integrated circuit including a PLL frequency synthesizer comprising:

a phase comparator unit;

a loop filter which receives an output of the phase comparator unit; and

a voltage control oscillator which receives an output of the loop filter,

the phase comparator unit comprising:

a reference signal frequency dividing unit which divides a frequency of a reference signal to generate a reference frequency divided signal;

a comparison signal dividing unit which divides a frequency of an output signal of the voltage control oscillator to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal;

a phase comparator which compares the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result;

a canceling signal generator which generates a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal;

a first initializing signal generator which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and

a second initializing signal generator which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving state canceling signal.

Claim 8 (Original): The semiconductor integrated circuit as claimed in claim 7, wherein frequency dividing rates used in the reference signal frequency dividing unit and in the comparison signal frequency dividing unit can be set independently of each other.

Claim 9 (Original): A transmitter-receiver including a PLL frequency synthesizer comprising:

a phase comparator unit;

a loop filter which receives an output of the phase comparator unit; and

a voltage control oscillator which receives an output of the loop filter,

the phase comparator unit comprising:

a reference signal frequency dividing unit which divides a frequency of a reference signal to generate a reference frequency divided signal;

a comparison signal dividing unit which divides a frequency of an output signal of the voltage control oscillator to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal;

a phase comparator which compares the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result;

a canceling signal generator which generates a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal;

a first initializing signal generator which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and

a second initializing signal generator which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving state canceling signal.

Claim 10 (Original): The transmitter-receiver as claimed in claim 9, wherein frequency dividing rates used in the reference signal frequency dividing unit and in the comparison signal frequency dividing unit can be set independently of each other.

Claim 11 (New): A method of controlling a power saving operation for a phase comparator unit, comprising the stops of:

dividing a frequency of an input signal to generate a comparison frequency divided signal, a phase of which is to be compared with a phase of the reference frequency divided signal;

comparing the phase of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result;

generating a power saving state canceling signal with the reference frequency divided signal so as to output a comparison result; and

generating an initializing signal for initializing the dividing the frequency of the reference signal or the frequency of the input signal in accordance with the power saving state canceling signal.